IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Original) A circuit apparatus with General Purpose Input Output (GPIO) pins, comprising:

a memory, which has a memory pin and is refreshed by a recharging signal to maintain stored data in the memory;

a control processing unit having a data pin, wherein the data pin is coupled to the memory pin; and

a buffer, coupled to the data pin, for receiving an input signal and feeding the input signal into the control processing unit according to a control signal synchronized with the recharging signal.

2. (Original) The circuit apparatus with General Purpose Input Output (GPIO) pins according to claim 1, wherein the control processing unit is an Application Specific Integrated Circuit (ASIC).

3. (Original) The circuit apparatus with General Purpose Input Output (GPIO) pins according to claim 1, wherein the buffer's model is 74HC/HCT244.

4. (Original) The circuit apparatus with General Purpose Input Output (GPIO) pins according to claim 1, wherein the memory is a Dynamic Random Access Memory.

5. (Original) The circuit apparatus with General Purpose Input Output (GPIO) pins according to claim 1, wherein the control signal is sent from the control processing unit.

6. (Original) A circuit apparatus with General Purpose Input Output (GPIO) pins, comprising:

a memory, which has a memory pin and is refreshed by a recharging signal to maintain stored data in the memory;

a control processing unit having a data pin, wherein the data pin is coupled to the memory pin; and

a buffer, coupled to the data pin, for outputting an output signal from the control processing unit, wherein the buffer outputs the output signal according to a control signal synchronized with the recharging signal.

7. (Original) The circuit apparatus with General Purpose Input Output (GPIO) pins according to claim 6, wherein the control processing unit is an Application Specific Integrated Circuit (ASIC).

8. (Amended) The circuit apparatus with General Purpose Input Output (GPIO) pins according to claim 6, wherein the buffer's model is ~~TC74/HC374~~ TC74HC374.

9. (Original)The circuit apparatus with General Purpose Input Output (GPIO) pins according to claim 6, wherein the memory is a Dynamic Random Access Memory.

10. (Original)The circuit apparatus with General Purpose Input Output (GPIO) pins according to claim 6, wherein the control signal is sent from the processing unit.